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(71) Applicant: KONINKLIJKE PHILIPS ELECTRONICS N.V. [NL/NL]; Groenewoudseweg 1, NL–5621 BA Eindhoven (NL).

(71) Applicant *(for SE only)*: PHILIPS NORDEN AB [SE/SE]; Kottbygatan 7, Kista, S–164 85 Stockholm (SE).

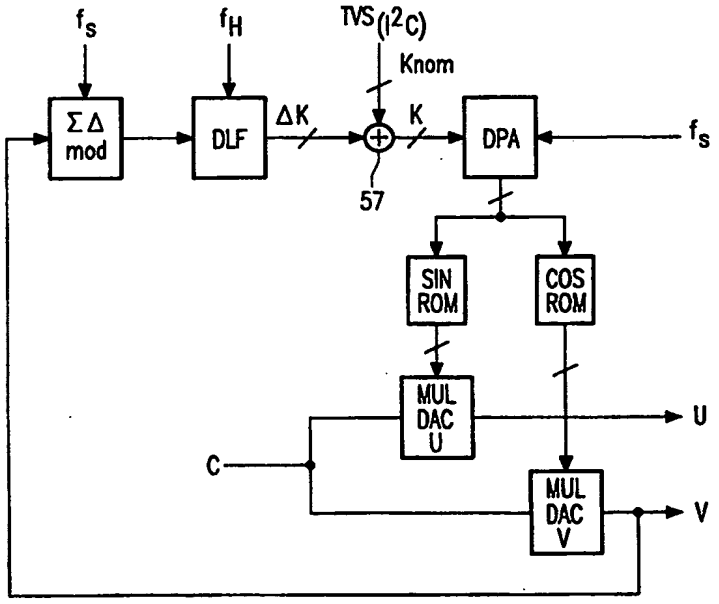
(72) Inventors: WISSING, Roy, Wilhelmus, Bernardus; Prof. Holstlaan 6, NL–5656 AA Eindhoven (NL). VAN LAMMEREN, Johannes, Petrus, Maria; Prof. Holstlaan 6, NL–5656 AA Eindhoven (NL). PELGROM, Marcellinus, Johannes, Maria; Prof. Holstlaan 6, NL–5656 AA Eindhoven (NL).

(74) Agent: STEENBEEK, Leonardus, J.; Internationaal Octrooibureau B.V., P.O. Box 220, NL–5600 AE Eindhoven (NL).

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(57) Abstract

In a method of demodulating an analog chrominance signal (C), digital quadrature signals are generated (DPA, SIN ROM, COS ROM) for demodulating (MUL DAC U, MUL DAC V) the analog chrominance signal (C) to obtain analog demodulated color difference signals (U, V). A digital phase error signal is furnished (ΣΔ mod) from at least one (V) of the analog demodulated color difference signals (U, V). The digital phase error signal is digitally filtered (DLF) to obtain a phase control signal (K) for the digital quadrature signals generation (DPA, SIN ROM, COS ROM).

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Color decoding.

The invention relates to a method and device for color decoding, and to a television signal display apparatus (TV set, PC having TV signal processing functions, etc.) comprising such a color decoding device.

Until now, multi-standard (PAL/NTSC) color decoding without digitizing the chrominance signal has mainly been done using an analog phase-locked loop, in which a voltage controlled crystal oscillator (VCXO) is locked to the color burst signal, see J. van Lammeren et al., Multi-Standard Video Front End, IEEE Transactions on Consumer Electronics, Vol. 37, No. 3, August 1991, pp. 190-196. A simplified diagram of a prior art analog color decoder is given in Fig. 1. The voltage controlled crystal oscillator VCXO regenerates sine and cosine versions of the color subcarrier, both with the correct phase. The subcarrier signals are fed to analog multipliers, where they are multiplied with the chrominance signal. By these multiplications, the chroma quadrature components U and V are separated and demodulated. The main disadvantage of this type of color decoder is that for each variant of the PAL/NTSC standards a different external crystal is necessary. Therefore a conventional multi-standard color decoder IC has to be equipped with several well-tunable external crystals, and thus with several additional IC pins.

In Murayama et al., Single-Chip BICMOS Multistandard Video Processor, IEEE Transactions on Consumer Electronics, Vol. 42, No. 3, August 1996, pp. 739-749, a color decoder is described that uses only one external crystal for decoding all variants of the PAL/NTSC standards. However, that system has some disadvantages:

- The external crystal that is used in this system still has to be a well-tunable one. Tunable crystals are much more expensive than standard crystals, which are very badly tunable.
- As the crystal oscillator (VCXO) in this system is locked to the incoming color burst, it can not at the same time be used as an asynchronous clock generator for other on-chip applications e.g. teletext decoding or A/D and D/A conversion.
- The system contains an analog PLL that acts as a bandpass filter for the

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digitally generated subcarrier. The performance of the VCO in this PLL completely determines the overall quality of the color decoder. The required specifications for this VCO can only be achieved when using a well-characterized process (e.g. BiCMOS) and will be degraded by the presence of digital circuitry on the chip, that cause substrate noise. As there is a trend towards CMOS processes and more and more digital functionality, this color decoder is not fully 'future proof'.

- The automatic phase control (APC) loop still requires an external loop filter, which costs an extra IC pin.

It is, *inter alia,* an object of the invention to provide a better multi-standard color decoding. To this end, a first aspect of the invention provides a method as defined in claim 1. A second aspect of the invention provides a quadrature signal demodulator as defined in claim 6. A third aspect of the invention provides a television signal display apparatus (TV set, PC having TV signal processing functions, etc.) comprising such a demodulator as a color decoding device. Advantageous embodiments are defined in the dependent claims.

In a method of demodulating an analog chrominance signal in accordance with a primary aspect of the present invention, digital quadrature signals are generated for demodulating the analog chrominance signal to obtain analog demodulated color difference signals. A digital phase error signal is furnished from at least one of the analog demodulated color difference signals. The digital phase error signal is digitally filtered to obtain a phase control signal for the digital quadrature signals generation.

These and other aspects of the invention will be apparent from and elucidated with reference to the embodiments described hereinafter.

In the drawings:

Fig. 1 shows a prior art color decoder;

Fig. 2 shows an embodiment of a color decoder in accordance with the present invention;

Fig. 3 shows an embodiment of a Sigma-Delta modulator for use in the embodiment of Fig. 2;

Fig. 4 shows an embodiment of a digital loop filter for use in the

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embodiment of Fig. 2; and

Fig. 5 shows an embodiment of a television display apparatus comprising the color decoder of Fig. 2.

A simplified diagram of a prior art analog color decoder is given in Fig. 1. The voltage controlled crystal oscillator VCXO regenerates a sin and a cos version of the color subcarrier, both with the correct phase. The subcarrier signals sin, cos are fed to analog multipliers MUL-U, MUL-V, where they are multiplied with a chrominance signal C. By these multiplications, the chroma quadrature components U and V are separated and demodulated. For each variant of the PAL/NTSC standards a different external crystal X1, X2, X3, X4 is present. Switches controlled by a TV standard indicating signal TVS connect the desired crystal to the oscillator VCXO. A color burst part CB of the chrominance signal C and the cos signal from the oscillator VCXO are applied to a phase detector PD, whose output is coupled to the oscillator VCXO through a loop filter LF.

A preferred embodiment of the present invention is a multi-standard color decoder that tackles all the disadvantages mentioned above. It concerns a mixed-signal system that needs only one (external) asynchronous crystal clock to demodulate all the variants of the PAL/NTSC color system, without digitizing the analog chrominance signal. For example, the clock signal already present for TXT processing can be used. Moreover, the system needs no additional external components/IC-pins and does not contain any highly critical analog modules. The loop filter can be made inside an IC. The decoder can therefore be realised in both BiCMOS and mainstream CMOS processes and can also be easily combined with digital functionality.

A block diagram of a preferred embodiment of the invention is given in Fig. 2. The heart of the system is formed by a digital phase accumulator DPA. It is used to generate the different subcarrier frequencies from a crystal-stable reference clock fs of e.g. 27 MHz. The principle of the phase accumulator, also called Discrete Time Oscillator (DTO), Direct Digital Synthesizer (DDS), or ratio-counter, is described in Murayama et al., Single-Chip BICMOS Multistandard Video Processor, IEEE Transactions on Consumer Electronics, Vol. 42, No. 3, August 1996, pp. 739-749, and in C.P. Sandbank, Digital Television, Wiley 1990. As the phase accumulator DPA generates a digital sawtooth of the desired subcarrier frequency, it is followed by two ROM tables SIN ROM and COS ROM that contain sine wave and cosine wave amplitude data. In this way the sawtooth is converted

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into both a sine and cosine waveform of which the spurious components are sufficiently suppressed. Moreover an excellent phase stability between sine and cosine is obtained. The digital subcarrier signals are multiplied with the analog chrominance signal C using two multiplying D/A converters MUL DAC U and MUL DAC V. These are D/A converters of which the reference input is controlled by an analog signal C instead of fixing it to a reference source. For example, a resistor string D/A converter with the resistance ladder controlled by a differential analog input, or a current D/A converter with binary weighted current sources controlled by a differential analog input. The analog output signals of the MUL DACs are the demodulated color difference signals U and V.

The digital subcarrier regenerator, formed by the phase accumulator DPA and the ROM look up tables SIN ROM and COS ROM, is locked to the incoming color burst by placing it in a phase-locked loop (PLL). During the burst key period, one of the MUL DAC's (MUL DAC V) acts as the phase detector for this PLL. The MUL DAC generates an analog phase error that is digitized by a simple first order 1-bit Sigma-Delta modulator $\Sigma\Delta$ mod operating at the system clock frequency fs of 27 MHz. The Sigma-Delta modulator is well known as an example of an attractive 1-bit A/D converter; alternatives are conceivable. The Sigma-Delta modulator is followed by a digital loop filter DLF that mainly operates at the TV line-frequency (fH). The digital filter DLF replaces the external loop filter of the analog color decoder and can also be easily combined with the decimation filter of the Sigma-Delta modulator. Besides, the digital loop filter DLF contains a PAL averager that eliminates the PAL H/2 burst swing. The digital output signal of the loop filter DLF is used to control the phase accumulator DPA, so it can remain in-lock with the color burst. The output signal of the loop filter DLF forms a small offset ΔK on the nominal input word Knom of the phase accumulator DPA. The nominal input word Knom is preset via the I2C bus and is determined by the color TV standard TVS to be received.

The preferred embodiment of Fig. 2 shows the following advantages. Instead of four tunable external crystals, an asynchronous crystal-stable system clock is used. The chrominance signal path remains analog. Instead of an external loop filter, an integratable digital loop filter is used. Highly critical analog components are avoided. Compared to the Murayama circuit having an analog PLL to adjust the clock frequency while the phase control signal K applied to the digital phase accumulator DPA is fixed, the preferred embodiment of the present invention features a digital PLL of which the phase control signal K is adjusted while the clock frequency is fixed so that, for example, the TXT clock can be used.

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Fig. 3 shows an embodiment of a Sigma-Delta modulator for use in the color decoder of Fig. 2. The analog signal from the MUL DAC V of Fig. 2 is applied to a first input of a subtracter 31, whose output is connected to a cascade connection of an integrator 33, a comparator 35, and a D flipflop 37 to obtain an output bitstream as the result of the 1-bit Sigma-Delta modulation. The output bitstream is applied to a second input of the subtracter 31 through a 1-bit D/A convertor 39, which may be formed by a switched current source. The integrator 33, the comparator 35, and the D flipflop 37 together perform a pulse-density modulation and a noise shaping function. The used Sigma-Delta modulator for digitizing the phase error has the following advantages. A dynamic range of 60 dB can easily be achieved in the frequency band of interest (0 - 7.8 kHz = 0.5 fH). It consists of very small and simple circuits, compared to a conventional A/D converter. Because of the high sampling frequency of 27 MHz, no analog pre-filter is required (a filtering would give response problems). Digital post-filtering can easily be combined with a loop filter.

Fig. 4 shows an embodiment of a digital loop filter DLF for use in the color decoder of Fig. 2. The bitstream supplied by the Sigma-Delta modulator of Fig. 3 is applied to an up/down counter 41 which is enabled by a burst gate signal and clocked by the high-frequency system clock, and which acts as decimation filter and as integrator of the PLL loop filter. The output of the counter is applied to a decimating D flipflop 43 clocked by a line frequency signal fH for providing a digitized and integrated phase error. The remainder of the loop filter of Fig. 4 takes care of the loop stability, gives the PLL desired parameters as to damping and natural frequency, provides a sufficient suppression of the PAL H/2 swing (> 45 dB), and limits the tuning range of the digital quadrature generator formed by the digital phase accumulator DPA and the sine and cosine ROMs to a range of about $\pm$ 600 Hz. The output of the D flipflop 43 is applied to a differentiator which comprises a multiplier 45, a D flipflop 47, and an adder 49 which adds the output of the D flipflop 47 to the output of the D flipflop 43. The output of the adder 49 is applied to a frequency range limiter 51. An output of the frequency range limiter 51 is applied to an averager which comprises a D flipflop 53, and an adder 55 which adds the output of the D flipflop 53 to the output of the frequency range limiter 51. The output of the adder 55 supplies the offset ΔK referred to with reference to Fig. 2. An adder 57, also shown in Fig. 2, adds this offset ΔK to the nominal value K which is determined by the TV standard. An output of the adder 57 is applied to a D flipflop 59 which furnishes the phase control signal K for the digital phase accumulator DPA of Fig. 2.

Fig. 5 shows an embodiment of a television display apparatus comprising

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the color decoder of Fig. 2. A television signal is received by an antenna A and applied to a tuner TUN which are carries out HF and IF demodulation functions to furnish a baseband video signal to a Y/C separator Y/C sep. The Y/C separator supplies a luminance signal Y to a luminance processor Y proc for carrying out functions like sharpness improvement etc. The separator supplies a chrominance signal C to the color decoder of Fig. 2 to obtain demodulated U and V signals. A matrix circuit MX converts the Y, U and V signals into R, G, and B color signals which are displayed on a display device D.

It should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be able to design many alternative embodiments without departing from the scope of the appended claims. In the claims, any reference signs placed between parentheses shall not be construed as limiting the claim. The invention can be implemented by means of hardware comprising several distinct elements, and by means of a suitably programmed computer.

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Claims:

1. A method of demodulating an analog chrominance signal (C), the method comprising the steps of:

generating (DPA, SIN ROM, COS ROM) digital quadrature signals;

demodulating (MUL DAC U, MUL DAC V) said analog chrominance signal (C) by means of said digital quadrature signals to obtain analog demodulated color difference signals (U, V);

furnishing ($\Sigma\Delta$ mod) a digital phase error signal from at least one (V) of said analog demodulated color difference signals (U, V); and

digitally filtering (DLF) said digital phase error signal to obtain a phase control signal (K) for said digital quadrature signals generating step (DPA, SIN ROM, COS ROM).

2. A method as claimed in claim 1, wherein said digital quadrature signals generating step (DPA, SIN ROM, COS ROM) comprises the steps of:

accumulating (DPA) said phase control signal (K) to obtain address signals; and

addressing look up tables (SIN ROM, COS ROM) by means of said address signals to obtain said digital quadrature signals.

3. A method as claimed in claim 1, wherein said demodulating step (MUL DAC U, MUL DAC V) includes the steps of applying said analog chrominance signal (C) to reference inputs of multiplying D/A converters having digital inputs coupled to receive said digital quadrature signals.

4. A method as claimed in claim 1, wherein said digital phase error furnishing step ($\Sigma\Delta$ mod) includes a 1-bit Sigma-Delta modulation of one (V) of said analog demodulated color difference signals (U, V).

5. A method as claimed in claim 1, wherein a fixed high frequency system clock (fs) is used to obtain said digital quadrature signals.

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6. A device for demodulating an analog quadrature modulated signal (C), the device comprising:

means for generating (DPA, SIN ROM, COS ROM) digital quadrature signals;

means for demodulating (MUL DAC U, MUL DAC V) said analog quadrature modulated signal (C) by means of said digital quadrature signals to obtain analog demodulated signals (U, V);

means for furnishing ($\Sigma\Delta$ mod) a digital phase error signal from at least one (V) of said analog demodulated signals (U, V); and

means for digitally filtering (DLF) said digital phase error signal to obtain a phase control signal (K) for said digital quadrature signals generating means (DPA, SIN ROM, COS ROM).

7. A television signal display apparatus, comprising:

means (Y/C sep) for generating luminance (Y) and chrominance (C) signals;

a device (Fig. 2) as claimed in claim 6 for demodulating an analog chrominance signal (C) to obtain analog demodulated color difference signals (U, V);

means (MX) for furnishing color signals (R, G, B) from said luminance signal (Y) and said analog demodulated color difference signals (U, V); and

means (D) for displaying said color signals (R, G, B).

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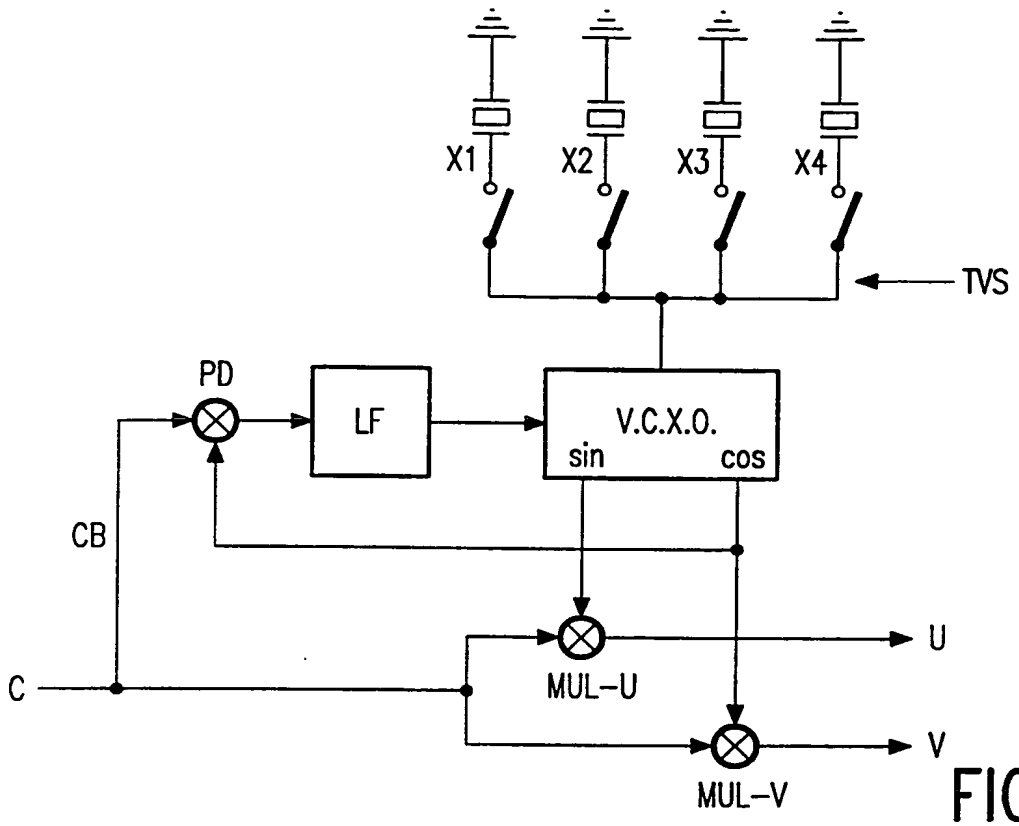


FIG. 1

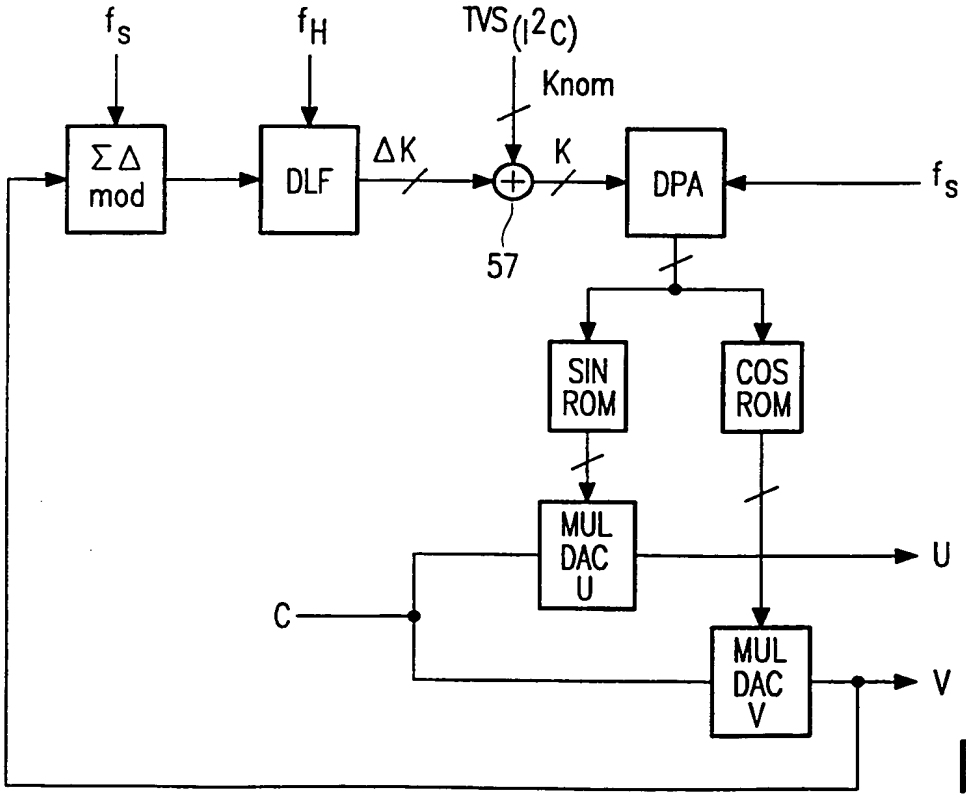


FIG. 2

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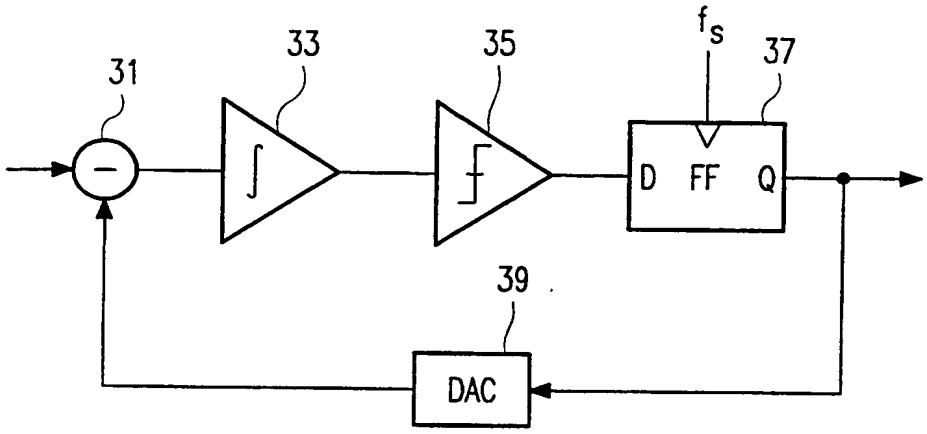


FIG. 3

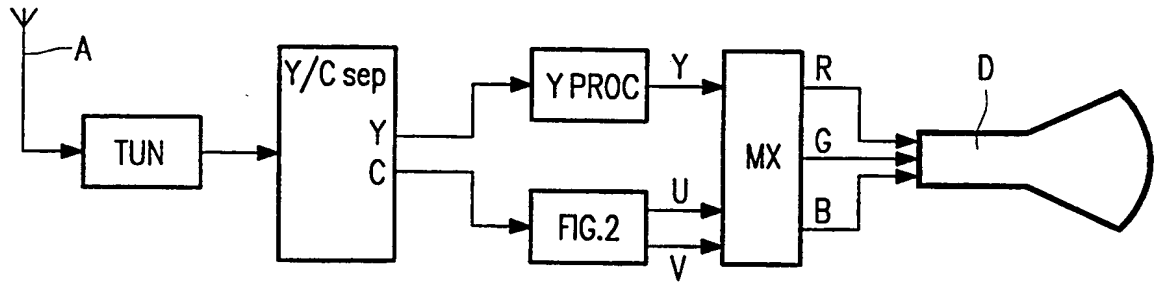


FIG. 5

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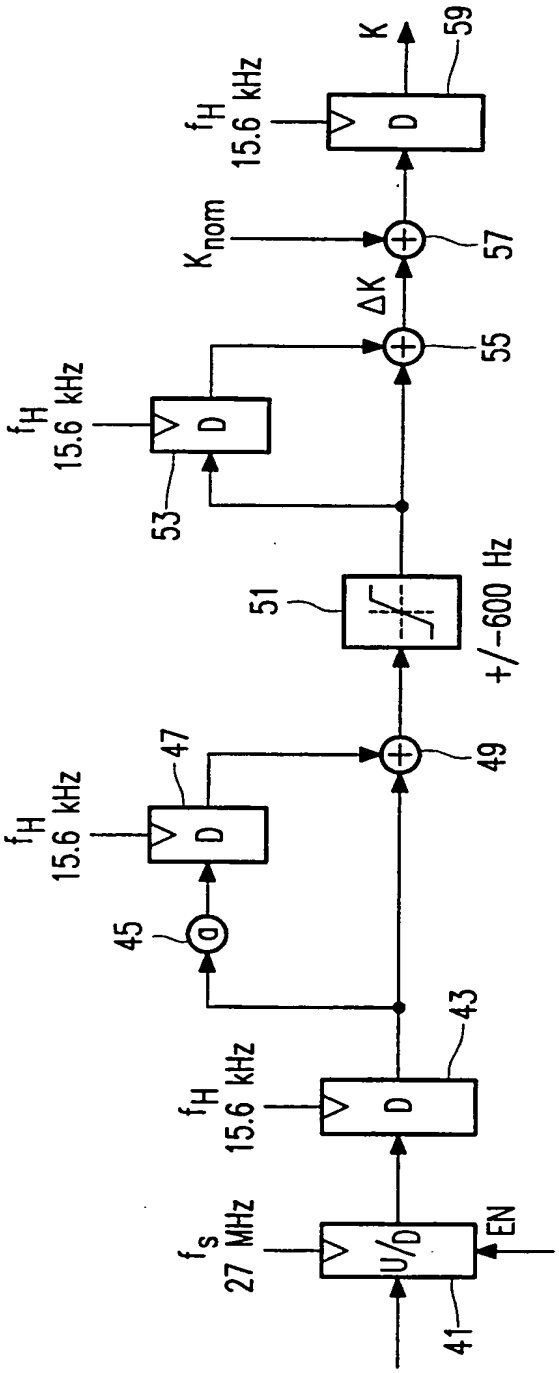


FIG. 4

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INTERNATIONAL SEARCH REPORT

International application No.
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A. CLASSIFICATION OF SUBJECT MATTER

IPC6: H04N 9/44, H04N 9/45, H04N 9/64 // H04N 11/16, H04N 11/14
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B. FIELDS SEARCHED

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Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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